DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-14, 18-24, drawn to Queuing arrangement, classified in class 370, subclass 412.

   II. Claims 15-17, drawn to fault recovery, classified in class 370, subclass 216-228.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different designs, modes of operation, and effects (MPEP § 802.01 and § 806.06). In the instant case, the different inventions , the invention I has separate limitations such as “A method for storing a packet in a shared memory in a packet switch, said shared memory comprising one or more buffers, each of said one or more buffers comprising a plurality of banks, said method comprising the step of: storing at least a portion of a packet in contiguous banks of a first buffer”. The invention II has separate limitations such as “A method for detecting a lost buffer in a shared memory of a packet switch, said method comprising the steps of: searching a free buffer list; and searching a cyclical trace memory”.

3. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply:

(a) the inventions have acquired a separate status in the art in view of their different classification;

(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

(d) the prior art applicable to one invention would not likely be applicable to another invention;

(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention**.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly

and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected invention.

If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

4. During a telephone conversation with Mr.Kevin M Mason on June 10, 2008 (Telephone No. 203-255-6560) a provisional election was made without traverse to prosecute the invention of I, claims 1-14, 18-24. Affirmation of this election must be made by applicant in replying to this Office action. Claims 15-17 have withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. This office action is in response to the Application SN 10/552,601 filed on 10/05/05. Claim 1-14, 18-24 are presented for examination.

Specification

1. This application does not contain an abstract of the disclosure as required by 37 CFR 1.72(b). An abstract on a separate sheet is required.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 10/07/05, 12/04/06 was filed . The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

3. Claim 2 is objected to because of the following informalities: “wherein said packet comprises a plurality of data units...if one said data units...said data unit" should be replaced by – wherein said packet comprises a plurality of portions…if one said portions…and said portions…is not a last portion of said packet ---. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. Claim 8 recites the limitation " wherein said sequential data units" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 4, 7, 9, 13, 14, 18, 21, 23, 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Muller et al. (Patent No.: 6,021,132)

Regarding to claim 1, Muller discloses a method for storing (figure 3A, col. 8, lines37-39, stored therein packets) in a shared memory (col. 8, lines 37-39, shared memory) in a packet switch (figure 2, switching fabric), said shared memory comprising one or more buffers (figure 3A, buffer #1, buffer #2, buffer #3), each of said one or more buffers comprising a plurality of banks (col. 8, lines 43-46, memory lines) (col. 8, lines 43-46, the buffers may be further subdivided into a number of memory lines. Each line may be used for storing packet data. In other embodiments, control information may also be associated with each of the memory lines. The control information may include information for facilitating efficient access of the packet data such as an end of packet field. The separation of control information and data increases the efficiency of accesses to and from the shared memory 230), said method comprising the step of:

- Storing at least a portion of a packet in contiguous banks of a first buffer (col. 8, lines 43-44, the buffers (buffer #1, #2, #3) may be further subdivided into the number of memory lines "bank") (col. 7, line 7, the a portion of the received

packet may be buffered temporarily at the input port 206 while a determination is made regarding the output port(s) 206 to which the packet is to be forwarded) (col. 8, lines 52-54, a given packet's data may be stored in one or more buffers, In this example, packet #1 (portions of packet #1) is distributed across three buffer 350-352), packet #2 (the portions of packet #2) is stored in three buffers 360-362, and packet #3 (the portions of packet #3) is fully contained within one buffer).

7. Regarding to claim 4, Muller et al. discloses wherein at least a portion (col. 7, line 7, portions of packet #1) (portions of packet #2) of each of two or more packets are stored in one of said buffers (figure 3A, 350, buffer #1 stored portions of packet #1) (figure 3A, 360, buffer #1 stored portion of packet #2) (figure 3A, 351, buffer #2 stored portions of packet #1) (figure 3A, 361, buffer #2 stored portions of packet #2).

8. Regarding to claim 7, Muller et al. discloses wherein said shared memory exchanges packets between ports (between input ports and output ports) in said packet switch (col. 7, lines 12-15, After a forwarding decision is received for a particular packet, the input port 206 transfers ownership of the one or more buffers corresponding to the packet to the appropriate output port(s) 206. The transfer of ownership includes the input port 206 notifying the shared memory manager 220 of the number of output ports 206 that should transmit the packet and the input port 206 forwarding the appropriate pointers to those output ports 206).

9. Regarding to claim 9, Muller et al. disclose a method for managing a share memory (figure 2, figure 3, shared memory 230, col. 8, lines 37-38, the shared memory 230 is depicted having stored therein packet data in a number of buffers), said shared memory comprising one or more buffers (figure 3A, buffer #1, buffer #2, buffer #3), said method comprising the step of:

Maintaining a buffer usage count for at least one of said buffers (Abstract, a shared memory manager for a packet forwarding device includes a pointer memory having stored therein information regarding buffer usage (e.g., usage counts) for each of a number of buffers in a shared memory) (col. 7, lines 25-27, The shared memory manager 220 then updates its internal counts used for tracking the number of buffer owners and returns the buffer to the free pool if appropriate (e.g., the buffer is no longer in any output queues)) (col. 9, lines 35-37, The buffer tracking unit 329 additionally includes a pointer random access memory (PRAM) 320. The PRAM 320 may be an on or off-chip pointer table that stores usage counts for buffers of the shared memory 230).

10. Regarding to claim 13, Muller et al. disclose the step of determining whether a buffer is free based on said buffer usage count (Abstract, a shared memory manager for a packet forwarding device includes a pointer memory having stored therein information regarding buffer usage (e.g., usage counts) for each of a number of buffers in a shared memory. An encoder is coupled to the pointer memory for generating an output which indicates a set of buffers that contains a free buffer. The shared memory manager

further includes a pointer generator that is coupled to the encoder for locating a free buffer in the set of buffers. The pointer generator is further configured to produce a pointer to the free buffer based upon the output of the encoder and the free buffer's location within the set of buffers) (col. 15, lines 66-67, col. 16, lines 1-3, wherein the step of dynamically allocating one or more buffers in a shared memory by determining one or more free buffer pointers further includes the step of updating a usage count corresponding to each of the one or more free buffer pointers).

11. Regarding to claim 14, Muller et al. disclose wherein said buffer usage count (Abstract, Usage count) provides an indication of the sum (Write) (col. 12, lines 30-31, the other two output ports 206 complete transmission of the buffer and so notify the buffer tracking unit 329 Write "SUM" = 0010b) over all packets in said at least one of said buffers of the number of output ports (two output ports) toward which each of said packet is destined (col. 12, lines 27-30, The buffer tracking unit 329 processes the input port's 0010b notification which indicates there are 3 buffer owners. Read: 1110b Modify: 1110b + 0011b + 0001b = 0010b Write: 0010b The other two output ports 206 complete transmission of 0010b the buffer and so notify the buffer tracking unit 329).

12. Regarding to claim 18, Muller et al. disclose a shared memory for storing a packet (col. 8, lines 38-39, shared memory 230 is depicted having stored therein packet data in a number of buffers), comprising:

- One or more buffers (figure 3A, Buffer #1, Buffer #2, Buffer #3), each of said buffers (Buffer #1, Buffer #2, Buffer #3) comprising a plurality of banks (memory lines) (col. 8, lines 43-46, the buffers may be further subdivided into a number of memory lines), wherein at least a portion of said packet (col. 8, lines 53-54, the portions of packet #1) is stored in contiguous banks of a first buffer (buffer #1) (col. 7, line 7, the a portion of the received packet may be buffered temporarily at the input port 206 while a determination is made regarding the output port(s) 206 to which the packet is to be forwarded) (col. 8, lines 52-54, a given packet's data may be stored in one or more buffers, In this example, packet #1 (portions of packet #1) is distributed across three buffer 350-352), packet #2 (the portions of packet #2) is stored in three buffers 360-362, and packet #3 (the portions of packet #3) is fully contained within one buffer).

13. Regarding to claim 21, claim 21 is rejected the same reasons of claim 4 above.

14. Regarding to claim 23, claim 23 is rejected the same reasons of claim 7 above.

15. Regarding to claim 24, Muller et al. disclose a counter for monitoring a buffer usage count (Abstract, Usage count) provides an indication of the sum (Write) over all packets in said at least one of said buffers of the number of output ports (two output ports) toward which each of said packet is destined (col. 12, lines 30-31, the other two output ports 206 complete transmission of the buffer and so notify the buffer tracking

unit 329 Write "SUM" = 0010b) (col. 12, lines 27-30, The buffer tracking unit 329 processes the input port's 0010b notification which indicates there are 3 buffer owners. Read: 1110b Modify: 1110b + 0011b + 0001b = 0010b Write: 0010b The other two output ports 206 complete transmission of 0010b the buffer and so notify the buffer tracking unit 329).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 2, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (Patent No: 6,021,132) in view of Benson et al. (Patent No.: 6,151,321).

Regarding to claim 2, Muller et al. disclose wherein said packet (packet #1) comprises a plurality of data units (portions of packet #1) , and further comprising the step of storing an portion of said packet in contiguous banks of second buffer (figure 3A, memory lines of buffer #2) if one of said data units (portions of packet #1) is stored in first buffer (buffer #1); however, Muller et al. are silent to disclosing said data unit stored in said last bank of said first buffer is not a last data unit of said packet.

Benson discloses the received shared memory pool mechanism 120 includes a first received shared memory pool 136 and second received shared memory pool 138.

Each receive shared memory pool has receive local buffers 122 (see col. 5, lines 40-42) (col. 5, line 48-49, two or more pools allows for the advantage of multiple bank typically built into memory device); comprising:

The step of storing an additional portion (the rest of the cell of the packet) of said packet in a second buffer (the second card buffer) if one of said data units (the cell of the packet) is stored in said first buffer (the first card buffer) and said data unit stored in said first buffer (the first card buffer) is not a last unit of said packet (figure 7B, place enough data in the first card buffer to fill the host buffer, place the rest of the cell into the second card buffer).

Both Muller and Benson disclose the shared memory. Benson recognizes storing an additional portion of said packet in a second buffer if one of said data units is stored in said first buffer and said data unit stored in said first buffer is not a last unit of said packet. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate storing an additional portion of said packet in a second buffer if one of said data units is stored in said first buffer and said data unit stored in said first buffer is not a last unit of said packet taught by Benson into the system of Muller in order to desire to utilize a dynamic packet memory management scheme to facilitate sharing of a common packet memory among all input / output ports for packet buffering (see Muller et al. col. 2, lines 16-17).

17. Regarding to claim 19, claim 19 is rejected the same reasons of claim 2 above.

18. Claims 3, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (Patent No: 6,021,132) in view of Kamaraj et al. (Patent No.: 6,501,757)

Regarding to claim 3, Muller et al. disclose one or more buffer in shared memory; one or more buffer comprising a plurality of banks (col. 8, line 43, the buffers may be further subdivided into a number of memory lines); however, Muller et al. are silent to disclosing wherein each of said one or more buffers comprises one or more group and each of said groups comprises a plurality of banks.

Kamaraj et al. disclose wherein each of said one or more buffers comprises one or more group and each of said groups comprises a bank (col. 7, lines 41-42, said cell buffer being housed in a shared cell buffer pool "buffer" organized as a bank of a plurality of groups.

Both Muller and Kamaraj disclose the shared memory in the switching device. Kamaraj recognizes wherein each of said one or more buffer comprises one or more groups. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate wherein each of said one or more buffers comprises one or more group and each of said groups comprises a bank taught by Muller into the system of Kamaraj in order to provide efficient implementation of internal queue while also allowing configurability of speeds (Kamaraj, col. 6, lines 52-53).

19. Regarding to claim 20, claim 20 is rejected the same reasons of claim 3 above.

20. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (Patent No: 6,021,132) in view of Beshai (Pub. No.: 2004/0184448).

Regarding to claim 5, Muller et al disclose each of said data port corresponding to one or more of said plurality of banks “buffers” (col. 8, lines 43-44, the buffers may be subdivided into a number of memory lines "banks") (col. 15, lines 1-2, a shared pool of packet memory and provides for efficient allocating of per port buffering that is proportional to the amount of traffic through a given port) ; however, Muller et al. are silent to disclosing the step of cyclically accessing one or more data ports.

Beshai discloses the step of cyclically accessing one or more data ports (page 1 paragraph [0005] the output rotor cyclically connects each transmit memory to each output port “data ports").

Both Muller and Beshai disclose the input ports, shared memory, and output ports. Beshai recognizes the step of cyclically accessing one or more data ports. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the step of cyclically accessing one or more data ports taught by Beshai into the sytem of Muller in order to desire to utilize dynamic packet memory management scheme to facilitate sharing of a common packet memory among all input / output ports for packet buffering (Muller, col. 2, lines 16-18).

21. Claims 6, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (Patent No: 6,021,132) in view of Lavelle et al. (Patent No.: US 6,812,929).

Regarding to claim 6, Muller et al. disclose allocating buffer in response to a buffer request (col. 10, lines 50-53, FIG. 5 is a flow diagram illustrating buffer allocation processing according to one embodiment of the present invention. At step 505, the next free buffer pointer is produced by the pointer generator 440. In one embodiment, the pointer generator 440 attempts to keep one or more pointers available to allow immediate servicing of buffer requests).

However, Muller et al. are silent to disclosing wherein said banks are divided into a first set of banks and a second set of banks, and a buffer that comprises one or more banks from said first set and a buffer that comprises one or more banks from said second set.

Lavelle et al. disclose wherein said banks are divided into a first set of banks and a second set of banks, and a buffer that comprises one or more banks from said first set and a buffer that comprises one or more banks from said second set (col. 14, lines 59-62, a frame buffer, wherein the frame buffer includes a first set of one or more banks, a second set of one or more memory banks).

Both Muller and Lavelle disclose the buffer and banks of the buffer. Lavelle recognizes wherein said banks are divided into a first set of banks and a second set of banks, and a buffer that comprises one or more banks from said first set and a buffer that comprises one or more banks from said second set. Thus, one would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate wherein said banks are divided into a first set of banks and a second set of banks, and a buffer that comprises one or more banks from said first set and a buffer that

comprises one or more banks from said second set taught by Lavelle into the system of the Muller in order to improve the efficiency of accesses to the frame buffer so that rendering accesses may be performed more quickly (Lavelle, col. 2, lines 53-54).

22. Regarding to claim 22, claim 22 is rejected the same reasons of claim 6 above.

23. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (Patent No: 6,021,132) in view of Sindhu et al. (Patent No.: US 6,493,347).

Regarding to claim 8, Muller et al. packets are stored in contiguous banks (col. 8, lines 43-44, buffers comprise number of memory lines) of at least one of said one or more buffers (figure 3A, buffer #1, buffer #2, buffer #3); however, Muller et al. are silent to disclosing wherein said sequential data units of said packet are stored in contiguous banks of at least one of said one or more buffers.

Sindhu et al. disclose wherein said sequential data units of said packet are stored in at least one of said one or more buffers (col. 22, lines 33-34, Let the cells generated by a given stream be numbered I, I +1, I +2, ….etc. As was described above, cells are written to sequentially increasing bank number I mod b) (Abstract, the distributed memory includes two or more memory banks, Each memory bank is used for storing uniform portions of a data packet received from source and linking information of a data packet to allow for the extraction of the uniform portions of a data packet from distributed location in memory in proper order).

Both Muller and Sindhu disclose the shared memory. Sindhu recognizes wherein said sequential data units of said packet are stored in at least one of said one or more buffers. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate wherein said sequential data units of said packet are stored in at least one of said one or more buffers taught by Sindhu into the system of Muller in order to allow the memory to be read and written conveniently (Sindhy, col. 4, line 9).

24. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (Patent No: 6,021,132) in view of Nation et al. (Patent No.: US 7,301,906).

Regarding to claim 10, Muller et al. disclose said buffer usage count by one to indicate that a packet destined for one output port is stored in said buffer (Abstract, a shared memory manager for a packet forwarding device includes a pointer memory having stored therein information regarding buffer usage (e.g., usage counts) for each of a number of buffers in a shared memory. An encoder is coupled to the pointer memory for generating an output which indicates a set of buffers that contains a free buffer. The shared memory manager further includes a pointer generator that is coupled to the encoder for locating a free buffer in the set of buffers. The pointer generator is further configured to produce a pointer to the free buffer based upon the output of the encoder and the free buffer's location within the set of buffers) (col. 15, lines 66-67, col. 16, lines 1-3, wherein the step of dynamically allocating one or more buffers in a shared memory by determining one or more free buffer pointers further includes the step of updating a usage count corresponding to each of the one or more free buffer pointers,

wherein the step of updating a usage count corresponding to the free buffer pointer comprises the step of setting the usage count to a predetermined value to accommodate a potential race condition in usage count processing.).

However, Muller et al. are silent to disclosing the step of incrementing said buffer usage count by one to indicate that a packet destined for one output port is stored in said buffer.

Nation et al. disclose the step of incrementing said buffer usage count by one to indicate that a packet destined for one output port is stored in said buffer (col. 10, lines 10-18, If the received packet is stored in buffer memory dedicated to the specific port, element 208 may therefore represent processing to increment a counter representing usage of preallocated, dedicated storage per port. If the received packet is stored in shared buffer memory, element 208 may therefore represent processing to increment a counter representing usage of shared storage per port and also decrementing a second counter representing available shared storage. Conversely, element 212 represents processing to increment or decrement appropriate counters indicating freeing of a previously allocated buffer either allocated as dedicated memory associated with the port or allocated from shared memory for temporary use by a particular port).

Both Muller and Nation disclose shared storage. Nation recognizes step of incrementing said buffer usage count by one to indicate that a packet destined for one output port is stored in said buffer. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate step of incrementing said buffer usage count by one to indicate that a packet destined for one output port is stored in

said buffer taught by Nation into the system of Muller in order to improve architecture in flow control and buffer memory management for high-speed serial communication devices to maintain high performance while reducing buffer memory requirements (col. 3, lines 46-47).

25. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (Patent No: 6,021,132) in view of Davis (Pub. No.: US 2007/0208876).

Regarding to claim 11, Muller discloses the step of decrementing (col. 12, lines 5-6, decremented) said buffer usage count (abstract, usage count) by one (col. 12, field count values) when a data unit is read from said buffer (col. 12, lines 7-20, the count field will accurately reflect the current number of output ports for the buffer pointer whether or not the count field was previously decremented by one or more output ports 206 as illustrated in Table 1, below. Table 1 illustrates the count field's value after each of the actions in the first column. An input port 206 requests a buffer pointer from the buffer 0000b tracking unit 329. A buffer pointer is provided to the input port 206. 1111b The forwarding decision indicates the packet including the 1111b buffer is to be forwarded to three output ports 206. The input port notifies the buffer tracking unit 329 of 1111b number of owners of the buffer and forwards the buffer pointer to each of the three output ports 206. One output port 206 completes transmission of the buffer 1111b and notifies the buffer tracking unit 329 that it no longer holds a copy of the buffer pointer. The buffer tracking unit 329 processes the output port's 1110b notification prior

to the input port's notification. Read: 1111b Modify: 1111b - 0001b = 1110b Write: 1110b The buffer tracking unit 329 processes the input port's 0010b notification which indicates there are 3 buffer owners. Read: 1110b Modify: 1110b + 0011b + 0001b = 0010b Write: 0010b).

However, Muller et al. are silent to disclosing said data unit is the last data unit of a packet.

Davis discloses the step of updating said buffer usage count (the usage buffer) by one when a data unit is read from said buffer and said data unit is the last data unit of a packet (end of the packet) (page 8 paragraph [0093] Buffer are allocated using a free buffer list……when a buffer is fall, or an end of packet is detected, the header queues corresponding to that packet are updated, as is information in the usage buffer…when the header queue is updated, the buffer entry in the usage buffer is updated with information from an FID RAM)

Both Muller and Davis disclose the step of updating said buffer usage count by one when a data unit is read from said buffer and said data unit is the last data unit of a packet. Thus, one would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the step of updating said buffer usage count by one when a data unit is read from said buffer and said data unit is the last data unit of a packet taught by Davis into the system of Muller in order to perform network monitoring without the use of additional probes (Davis, page 1 [0005]).

26. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (Patent No: 6,021,132) in view of Miller et al. (Patent No.: US 6,247,058)

Regarding to claim 12, Muller et al. discloses said buffer usage count (See abstract, Usage count); however, Muller et al. are silent to disclosing wherein said usage count indicate a number of destination port for a packet to perform a multicasting operation.

Miller et al. disclose wherein said usage count indicate a number of output port for a packet to perform a multicasting operation (col. 7, lines 43-45, When a broadcast or multicast packet is received, it is assigned a time stamp and stored in broadcast packet output buffer 98 along with a counter indicating the number of ports to which the packet is broadcast).

Both Muller and Miller disclose Buffer Usage Count. Muller recognizes wherein said usage count indicate a number of output port for a packet to perform a multicasting operation. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate wherein said usage count indicate a number of output port for a packet to perform a multicasting operation taught by Miller into the system of Muller in order to support a variety of packet management function (Miller, col. 1, line 10). The combined system would have been enable to handle additional traffic (col. 4, line 27).

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Oberman et al. (Pub. No.: US 2003/0026267).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHUONG T. HO whose telephone number is (571)272-3133. The examiner can normally be reached on 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, EDAN ORGAD can be reached on (571) 272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

06/14/08

/CHUONG T HO/

Temporary Grant of Partial Signatory Authority Examiner, Art Unit 2619